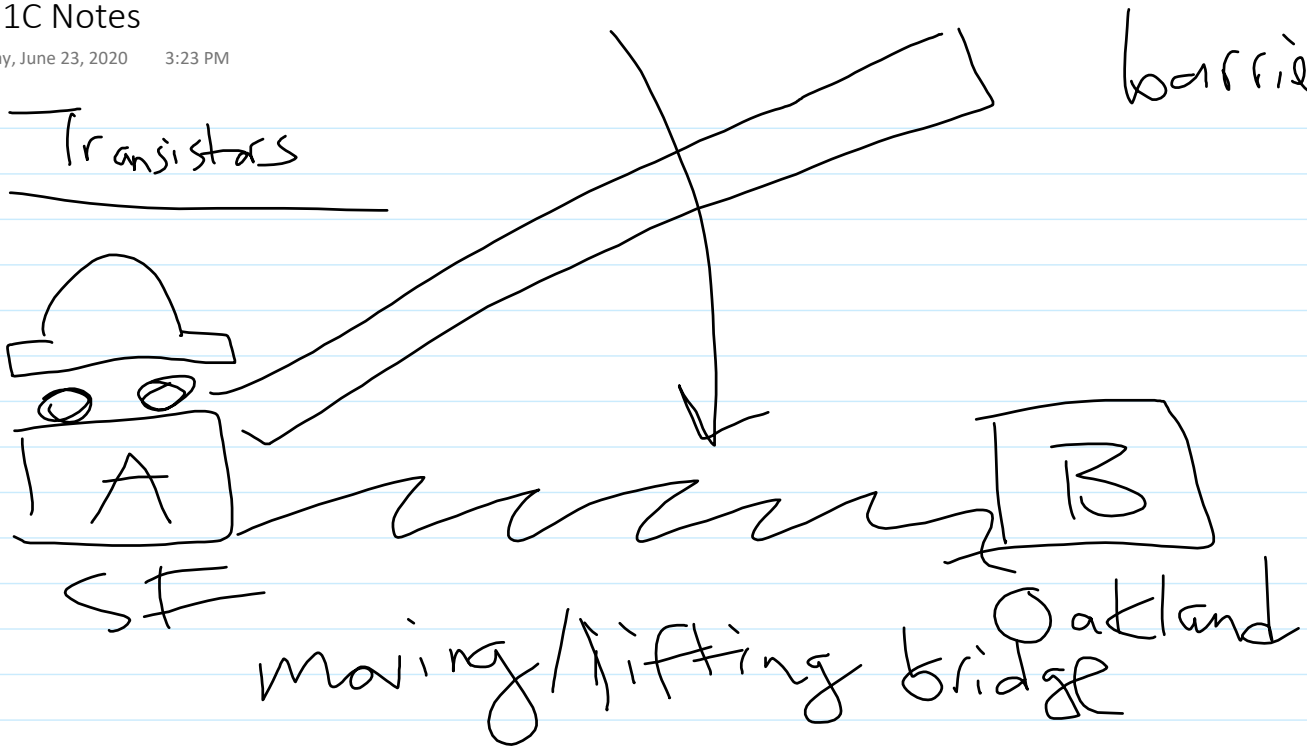
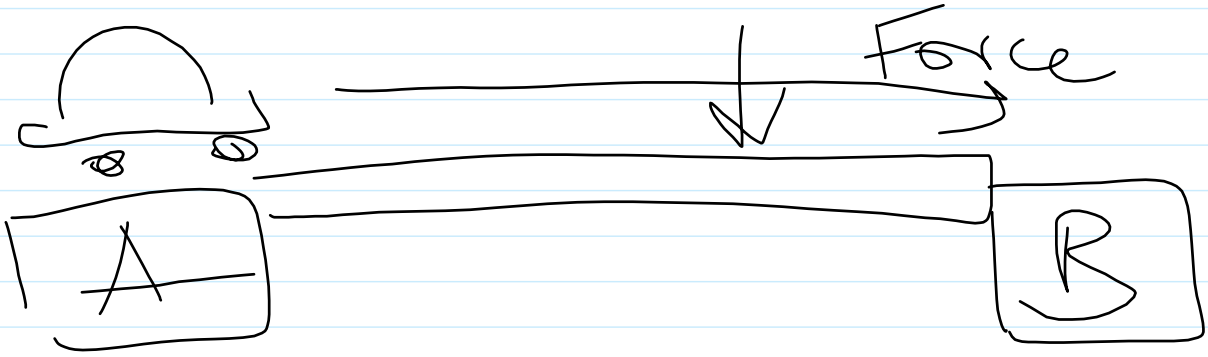
# Dis 1C Notes

Tuesday, June 23, 2020 3:23 PM

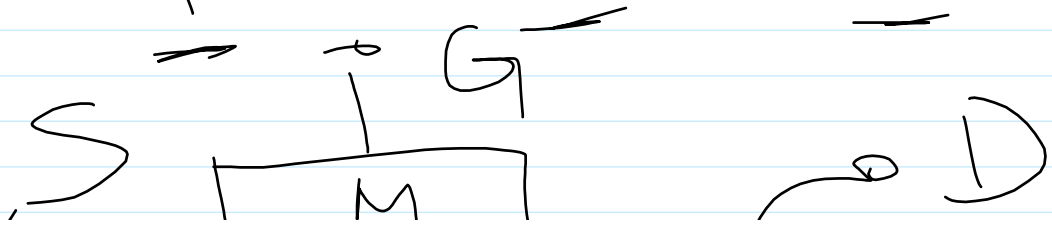


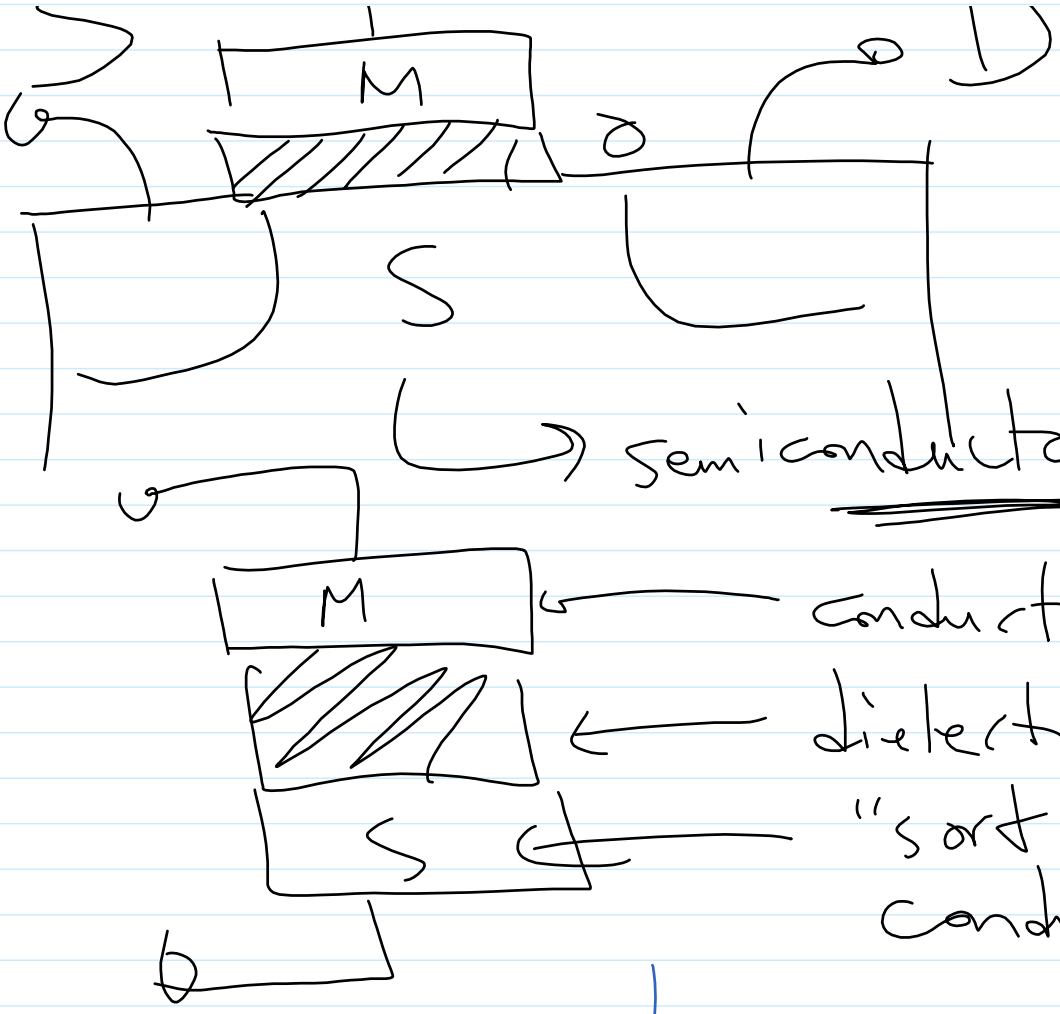




physical picture → IC model

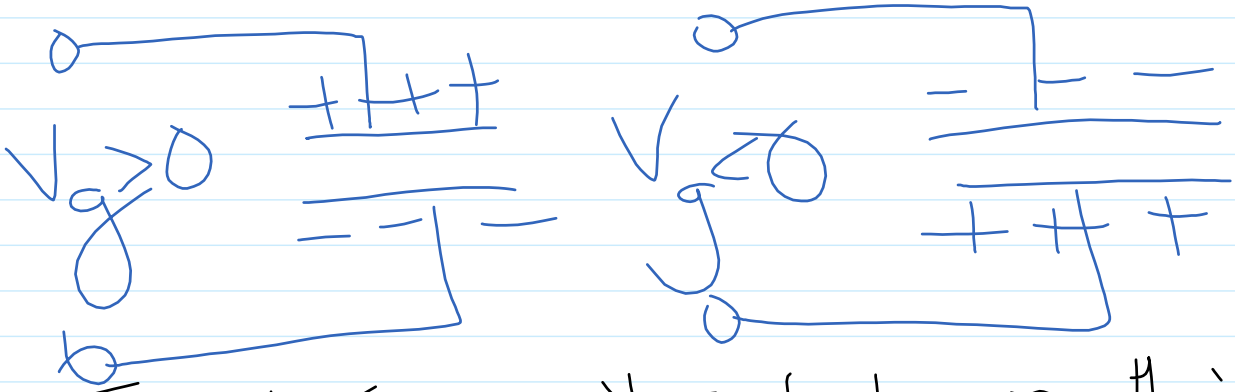
## MOSFET

Metal oxide semiconductor field-effect transistor



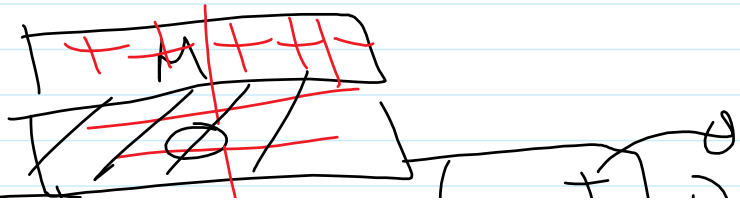


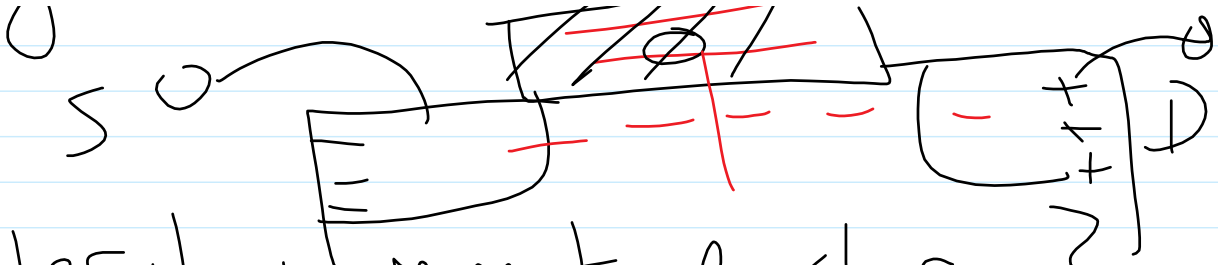

capacitor!




Transistor: similar but we think relative to $V_t$ (threshold voltage)

$V_{gs} > V_t$






lateral movement of charge?

Apply a voltage b/w D and S to push the charges along!

$V_{DS} > 0$

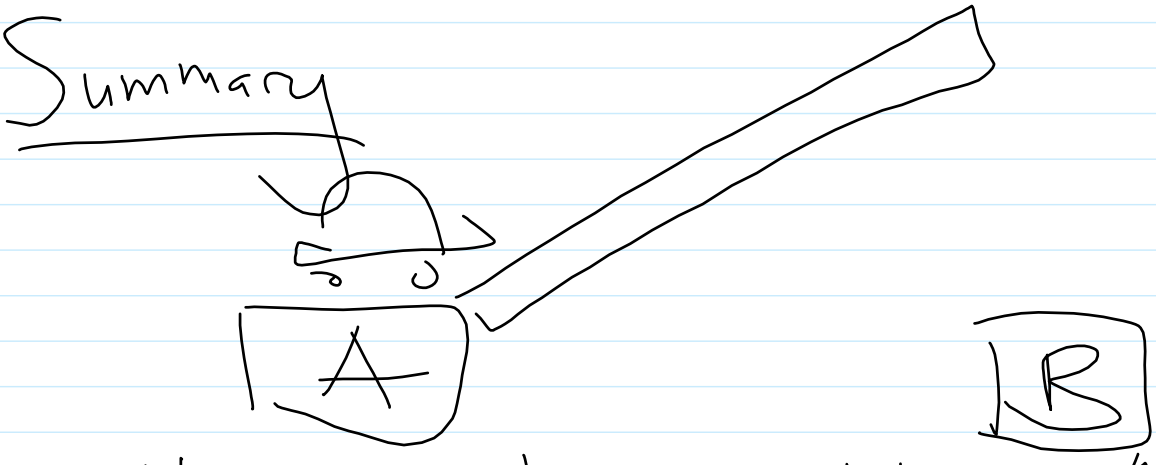
That was an "NMOS" transistor

→ why "N"?

negatively charged carrier

positive for PMOS

Summary



* $V_{GS}$ pushes the "bridge" down
* $V_{DS}$ pushes the "cars" (charges)

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physics ⟶ 16B model

16B

1. voltage-controlled switch
   (most ideal; helpful for digital logic)
2. resistor-switch model
   (helpful when thinking about power)
3. RC model
   (helpful for thinking about delays and transients)

$$i_C = C\frac{dV_c}{dt}$$

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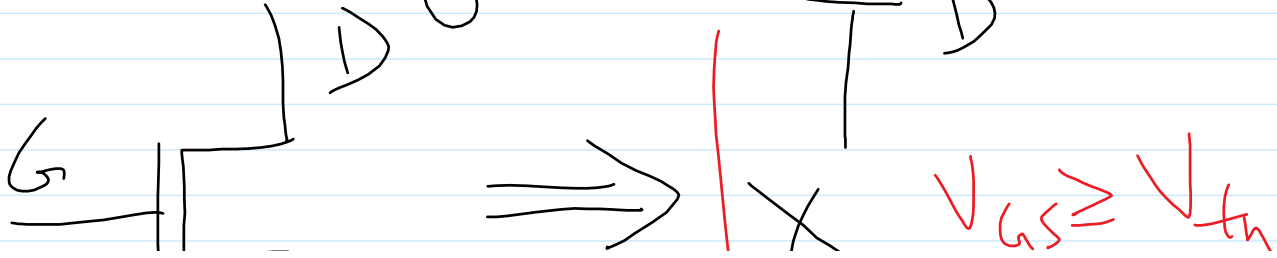
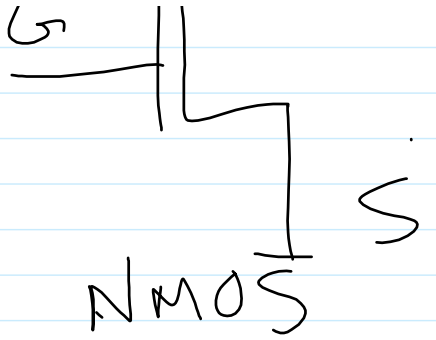
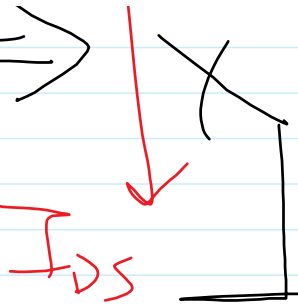
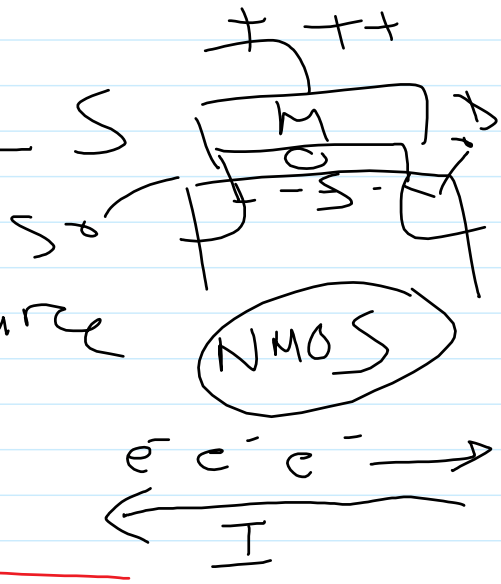
1. Voltage-controlled switch





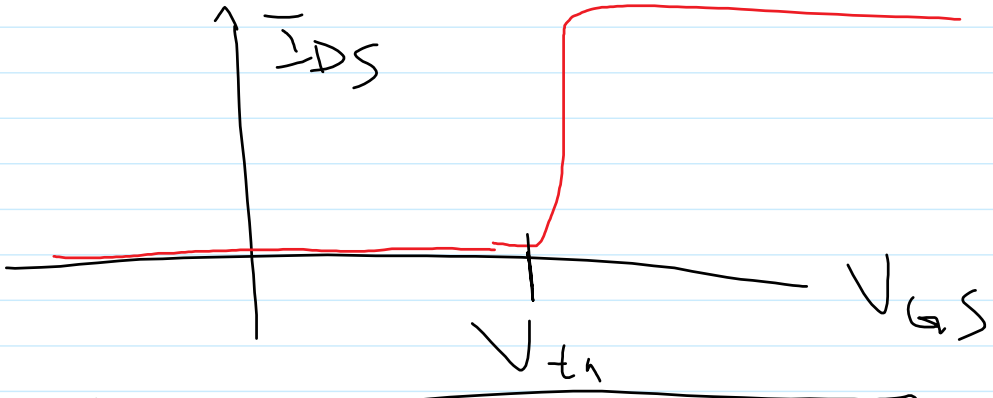




$I_{DS} = I$ drain to source

$V_{GS} = V_G - V_S$

$V_{DS} = V_D - V_S$



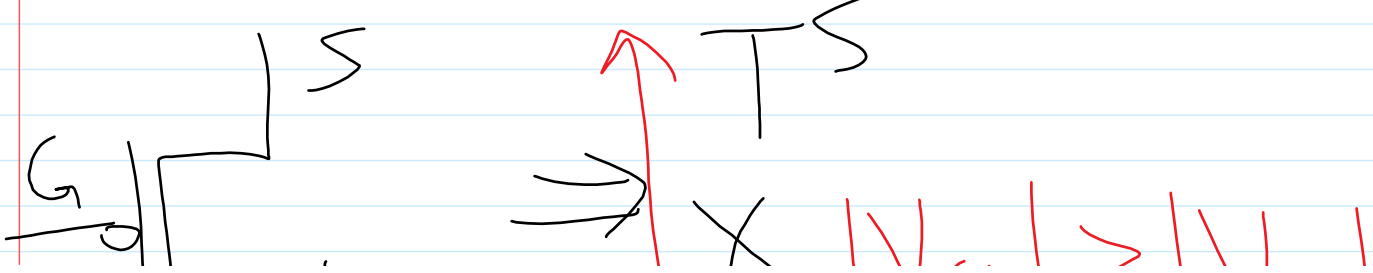

$I_{DS} > 0$ always

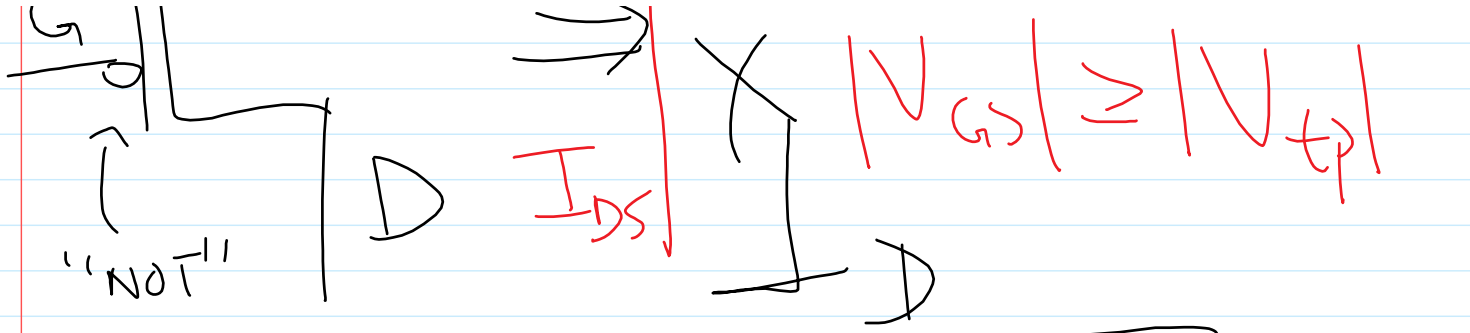
$V_{th} > 0$ usually

$V_{gs} \geq V_{th}$

NMOS

PMOS = "NOT" NMOS



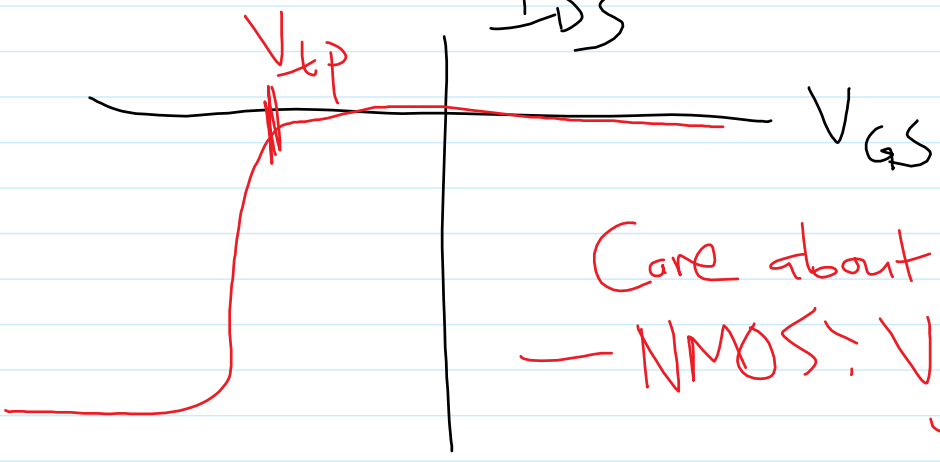



$V_{tp} < 0$ almost always

$I_{DS} < 0$ always

PMOS

$|V_{gs}| \geq |V_{tp}|$

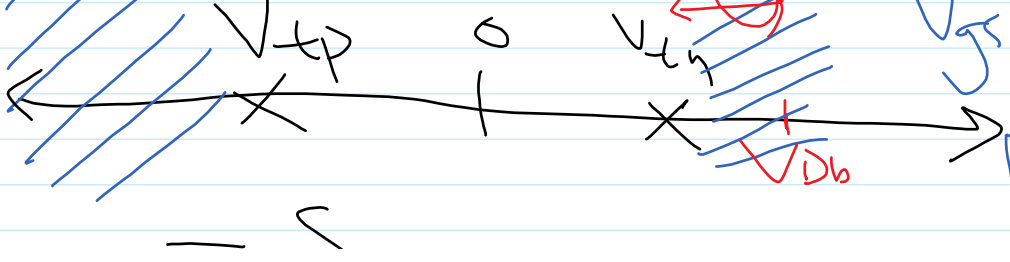



Care about the "delta":

— NMOS: $V_{gs}$ more positive than $V_{th}$

$V_{gs}$ that turn PMOS on

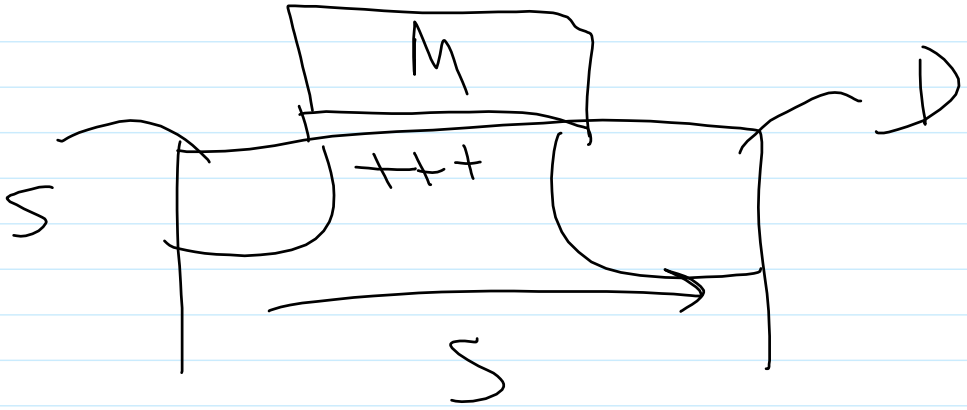
— PMOS: $V_{gs}$ more negative than $V_{tp}$




labelled direction of current

$I_{DS} < 0$ always

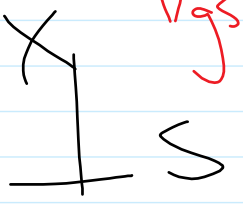
direction positive current is actually flowing



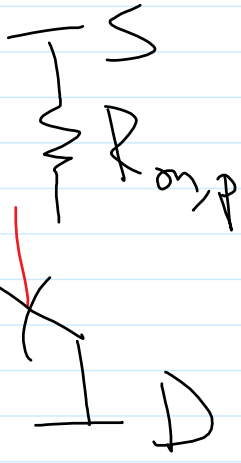

## II. Resistor Switch Model

NMOS


$V_{gs} \geq V_{tn}$

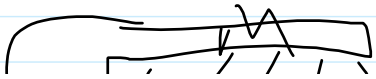



PMOS

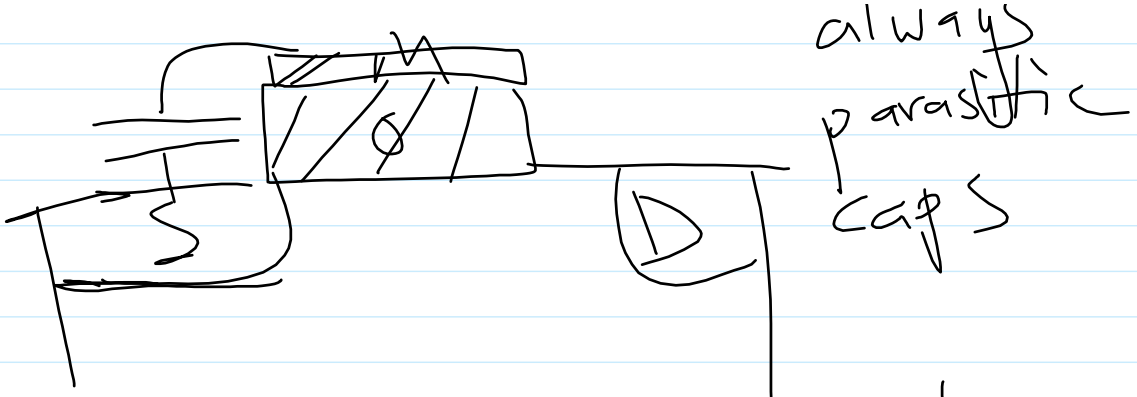



$|V_{gs}| \geq |V_{tp}|$

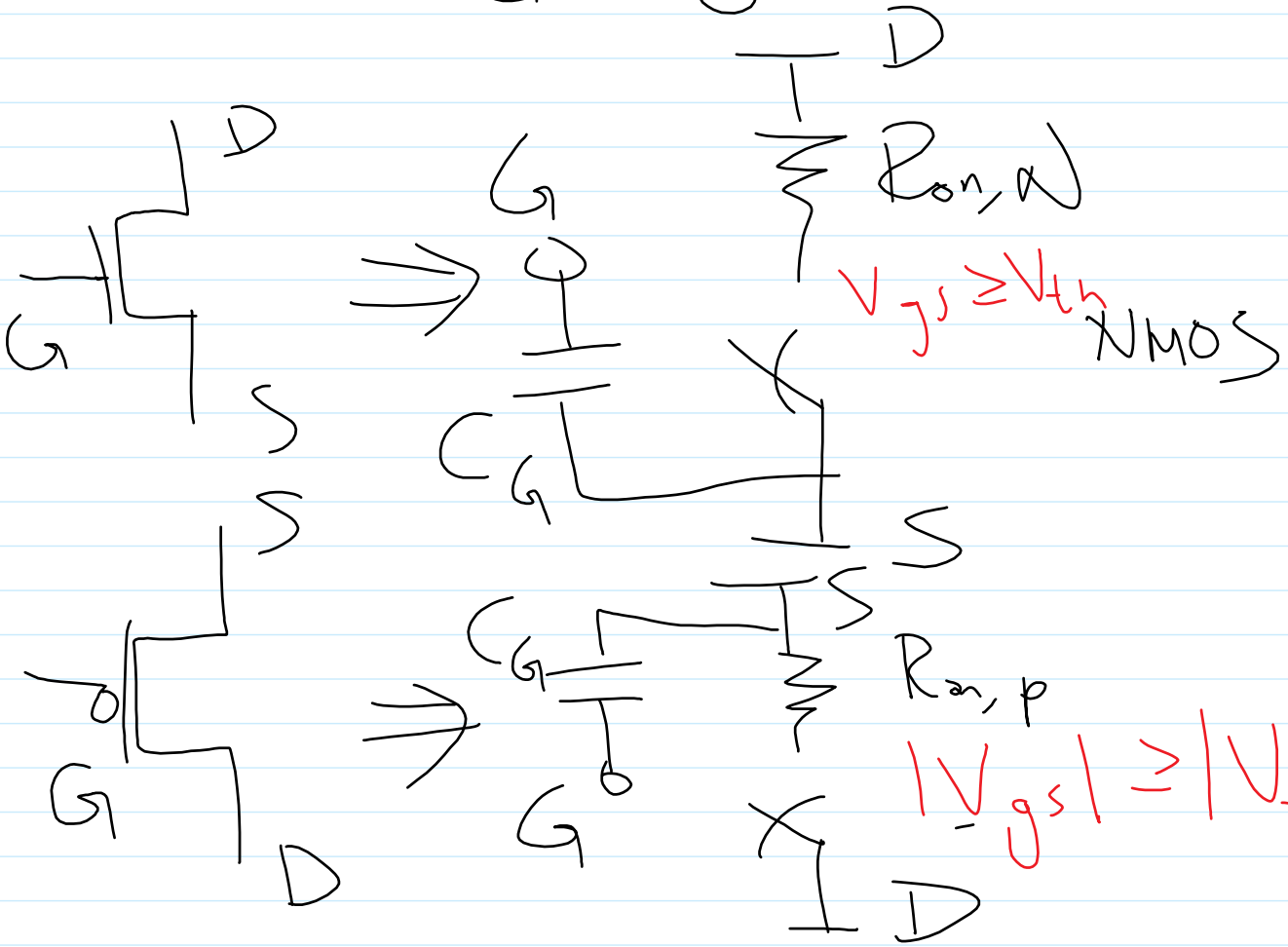
## III. RC model



always




$C_G$ = gate capacitance



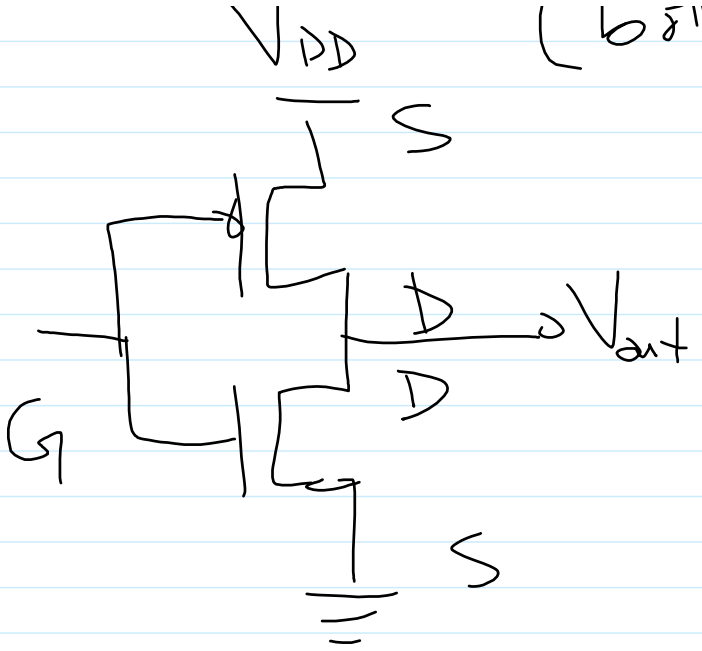

# IV. CMOS inverter

complementary (both NMOS and PMOS)

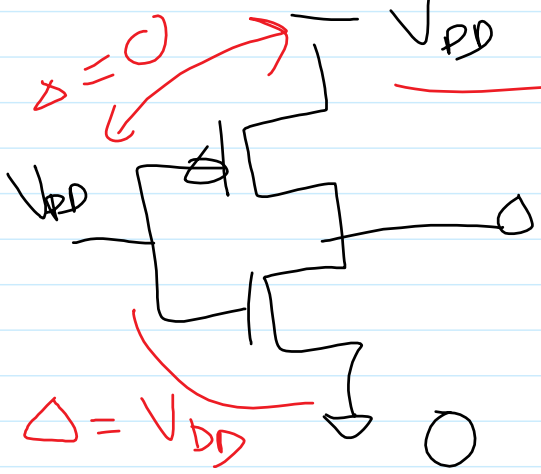
$V_{DD}$

(both NMOS and PMOS)

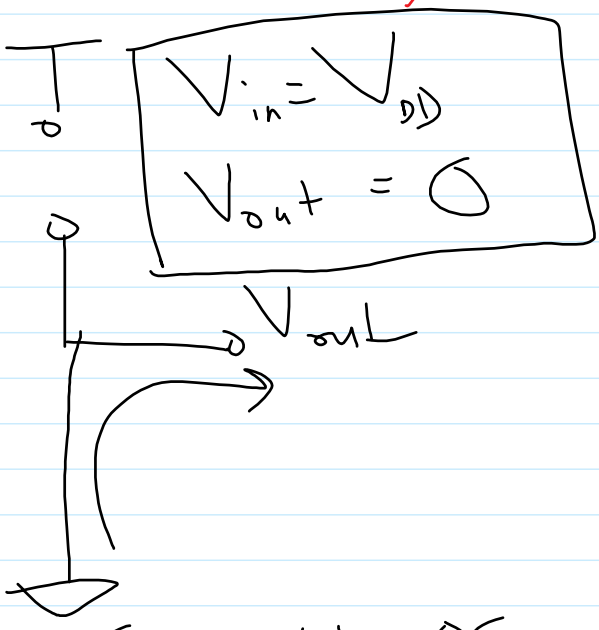
Use switch model.



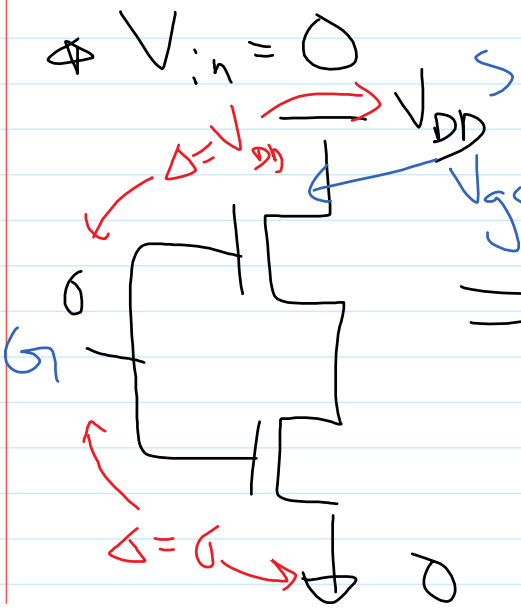

$V_{in} = V_{DD}$



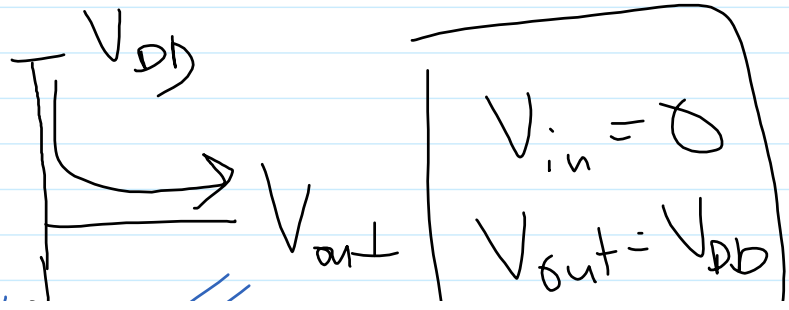

→ PMOS ~~off~~, NMOS on




$V_{in} = 0$



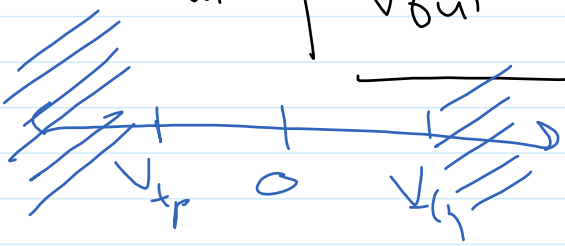

PMOS on, NMOS off



$\Delta = 0 \rightarrow t$ 0

$V_{gs}$ relative to $V_t$

$V_{out}$ | $V_{out} = V_{DD}$

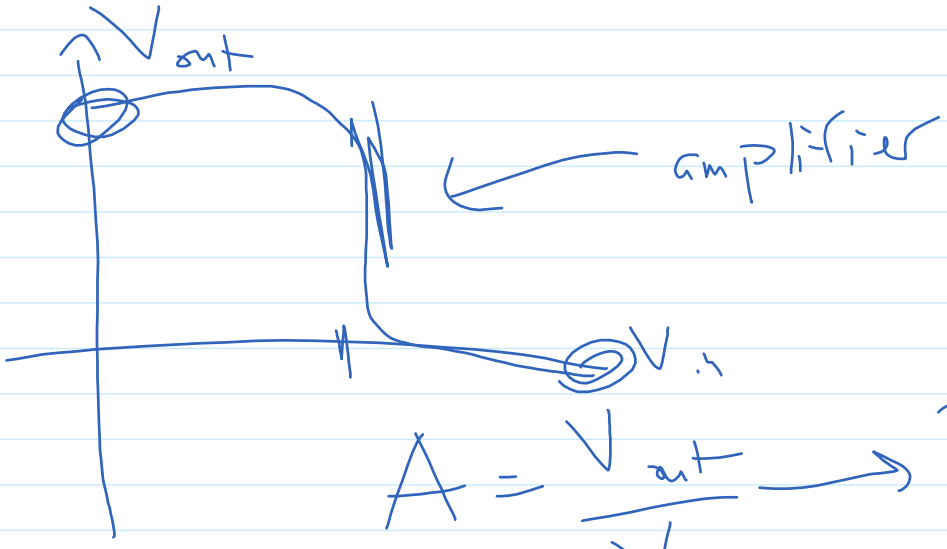



Truth Table

| $V_{in}$ | $V_{out}$ |
|---|---|
| 1 | 0 |
| 0 | 1 |

"0" → 0V

"1" → $V_{DD}$




$$A = \frac{V_{out}}{V_{in}} \rightarrow \frac{\partial V_{out}}{\partial V_{in}}$$

## 2 Single-transistor Inverter

Consider the following single-transitor inverter, consisting of an NMOS transistor and a resistor, where for $N_1$ we have $0 < V_{tn} < V_{DD}$.

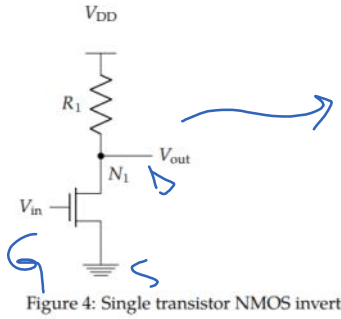



Figure 4: Single transistor NMOS inverter

a) Replace the transistor $N_1$ with a switch, the simplest model of a transistor and answer the following questions

(i) What is $V_{out}$ when $V_{in} = 0$?

(ii) What is $V_{out}$ when $V_{in} = V_{DD}$?

(iii) What is the power consumption of the circuit when $V_{in} = 0$? How about when $V_{in} = V_{DD}$

(i) $V_{in} = 0$

$V_{GS} = 0 - 0 = 0 < V_{tn}$

NMOS off

$I = 0$

$\Delta V = 0$

$V_{DD} - V_{out} = 0$

$V_{in} = 0, V_{out} = V_{DD}$

(ii) $V_{in} = V_{DD}$

$V_{GS} = V_{DD} - 0 = V_{DD} \geq V_{tn}$

NMOS is on

$V_{in} = V_{DD}, V_{out} = 0$

(iii) Power?

$V_{in} = 0$: $P = IV_{DD} = 0 \cdot V_{DD} = 0$

$P = 0$

$V_{in} = V_{DD}$: $I = \frac{V_{DD}}{R_1}$, $P = IV_{DD} = \frac{V_{DD}^2}{R_1}$

$V_{in} = V_{DD}$ ; $I = \frac{V_{DD}}{R_1}$ , $P = IV_{DD} = \frac{V_{DD}^2}{R_1}$

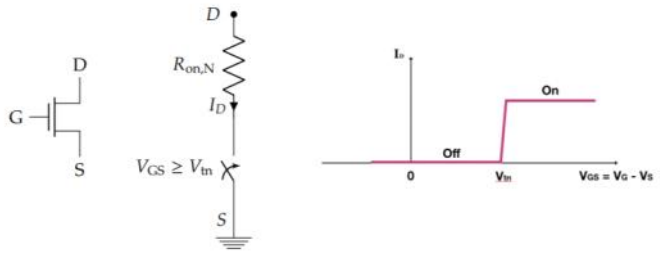



Figure 5: NMOS Transistor Resistor-switch model

b) Now replace the NMOS device with a transistor model that includes an internal resistor, such as the one in the figure above.

(i) What is $V_{out}$ when $V_{in} = 0$?

(ii) What is $V_{out}$ when $V_{in} = V_{DD}$ in terms of $R_1$ and $R_{on,N}$?
What is this value if $R_{on,N} = \frac{1}{10}R_1$?
How much power does the circuit consume?

(b) Resistor-Switch Model

(i) $V_{in} = 0$, $V_{GS} = 0 - 0 = 0 < V_{tn}$, NMOS off

$V_{DD}$ $R_1$ $R_{on,N}$

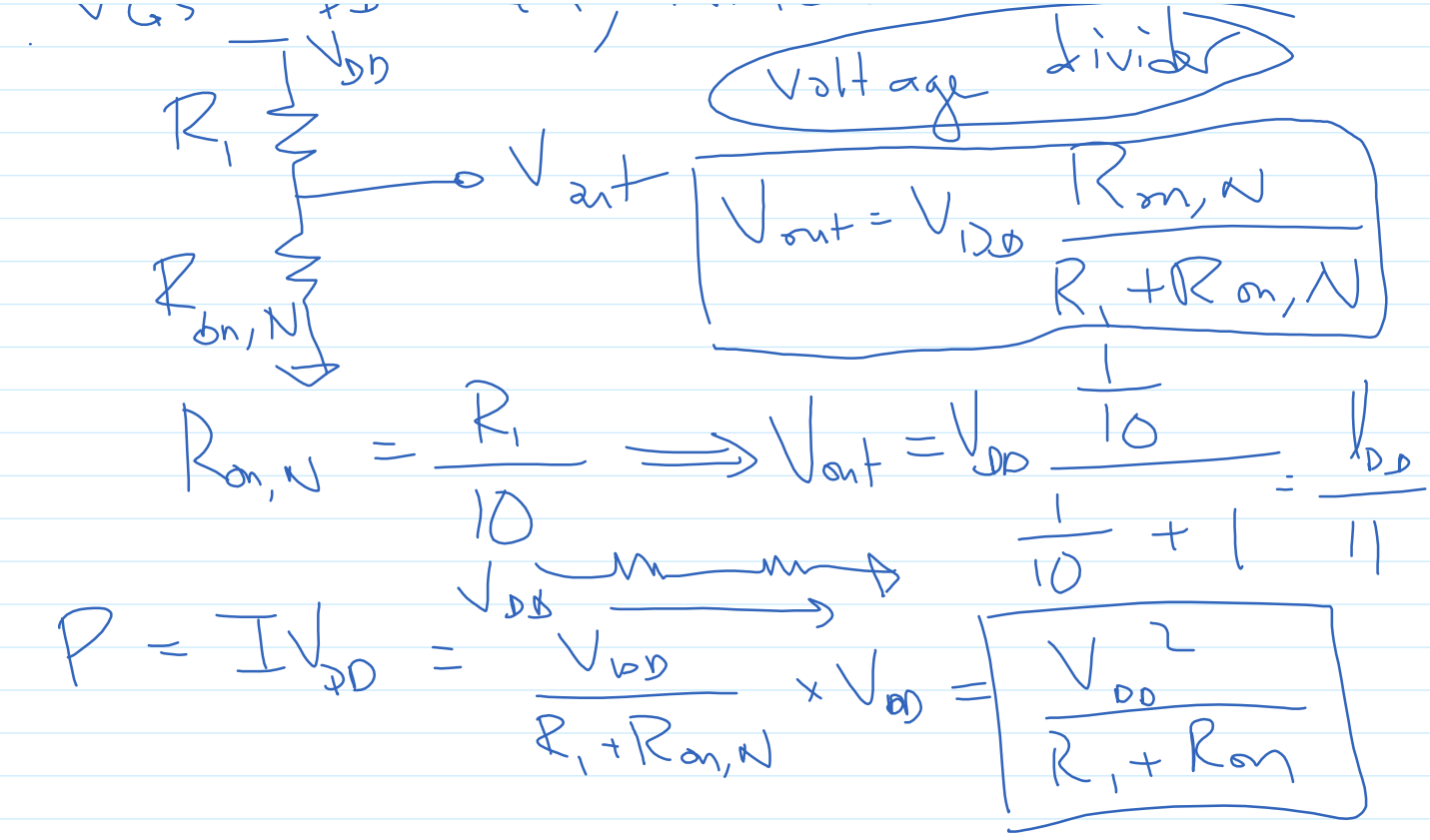
$V_{in} = 0$
$V_{out} = V_{DD}$
$P = 0$

(ii) $V_{in} = V_{DD}$

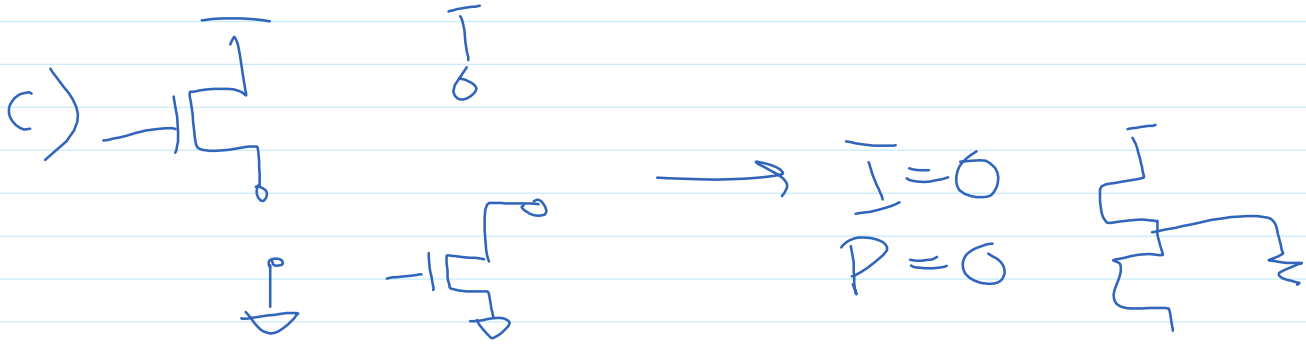
$V_{GS} = V_{DD} > V_{tn}$, NMOS on

$V_{DD}$

Voltage divider




c) Now consider a CMOS inverter with both PMOS and CMOS devices, such as that of Figure 3. How does the performance and power consumption compare?



## 3 NAND Circuit

Let us consider a NAND logic gate. This circuit implements the boolean function $\overline{(A \cdot B)}$.

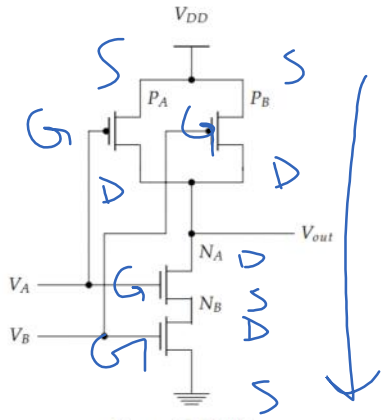



Figure 6: NAND

$V_{tn}$ and $V_{tp}$ are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

a) Label nodes.

gates — floating thingy

S/D: NMOS — $I_{DS} > 0$

positive current flows from D to S → $V_D > V_S$

PMOS — $I_{DS} < 0$

$V_S > V_D$

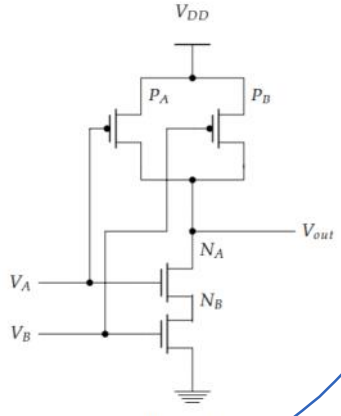



Figure 7: NAND

b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open circuits? Which transistors act like closed circuits? What is $V_{out}$?

c) If $V_A = 0V$ and $V_B = V_{DD}$, what is $V_{out}$?

d) If $V_A = V_{DD}$ and $V_B = 0V$, what is $V_{out}$?

e) If $V_A = 0V$ and $V_B = 0V$, what is $V_{out}$?

$\overline{(A \cdot B)}$ = not and = nand

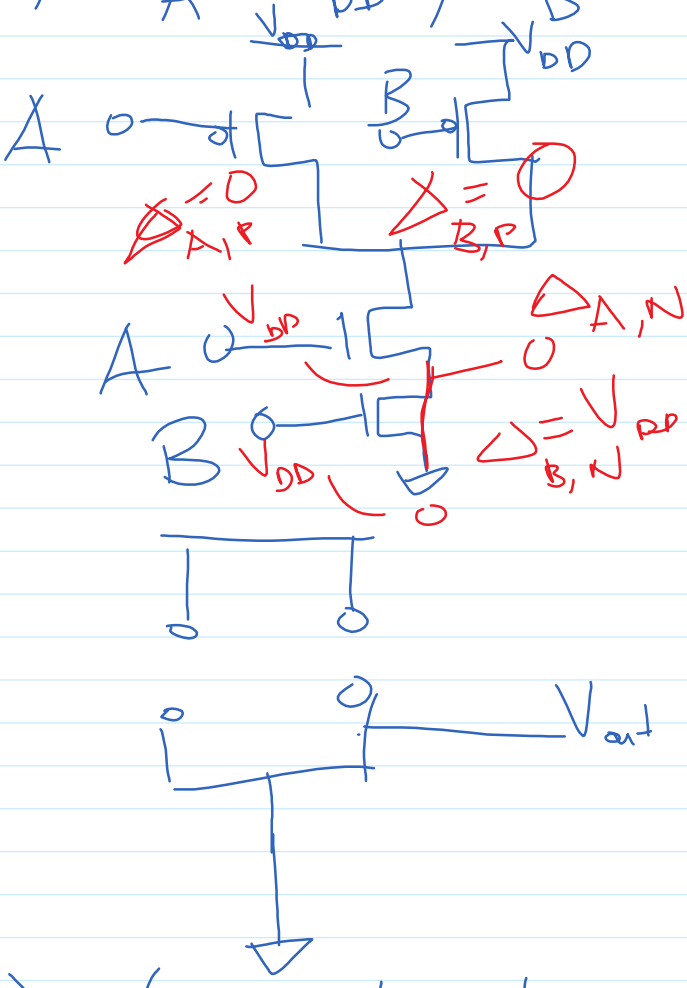
Expect

| A | B | Out |
|---|---|---|
| 1 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 0 | 1 |

a) $V_A = V_{DD}$ / $V_B = V_{DD}$

PMOS A R

a) $V_A = V_{DD}$, $V_B = V_{DD}$




→ PMOS A, B off

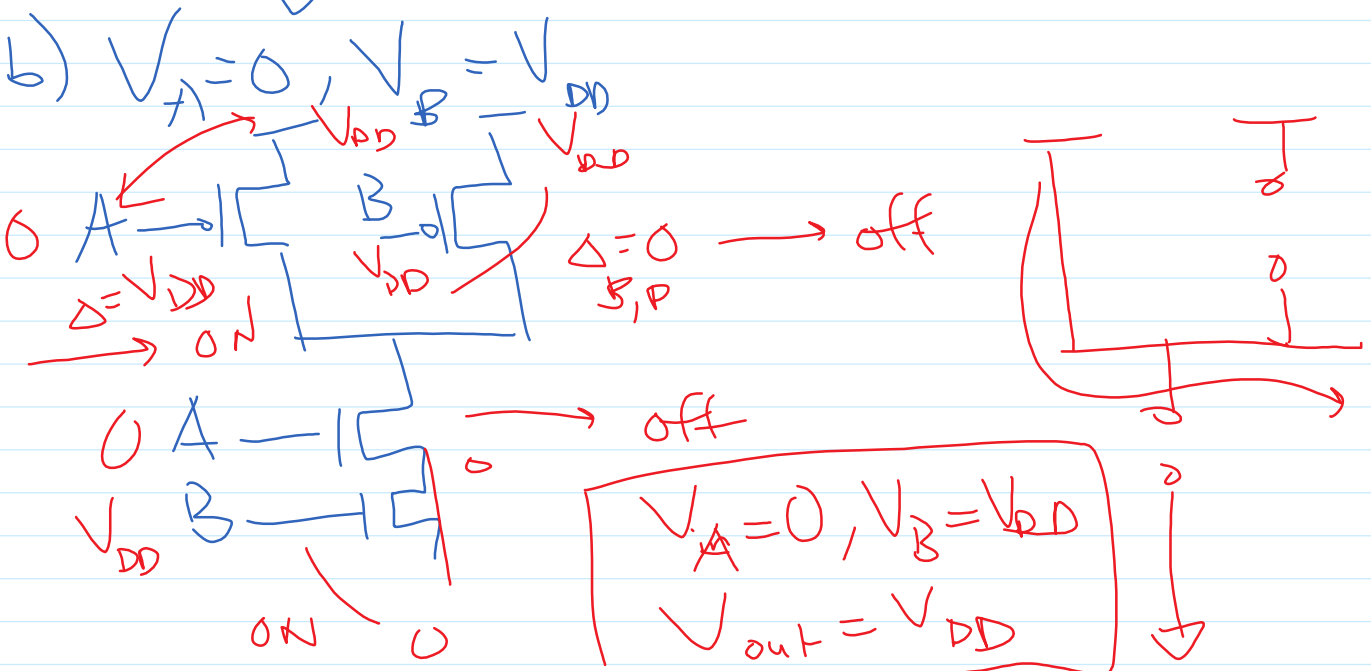
→ NMOS A, B on

$V_{out} = 0$

$V_A = V_{DD}$, $V_B = V_{DD}$

"1" "1"

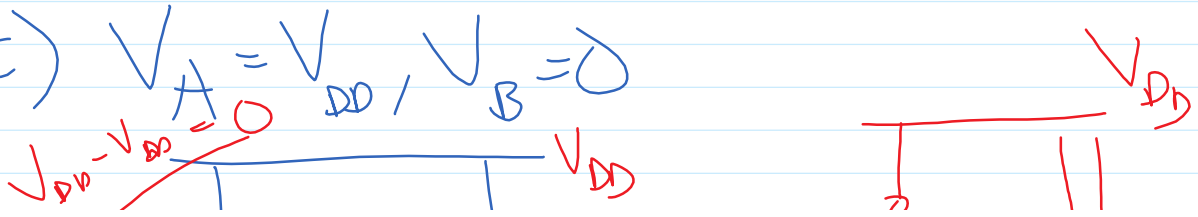
b) $V_A = 0$, $V_B = V_{DD}$

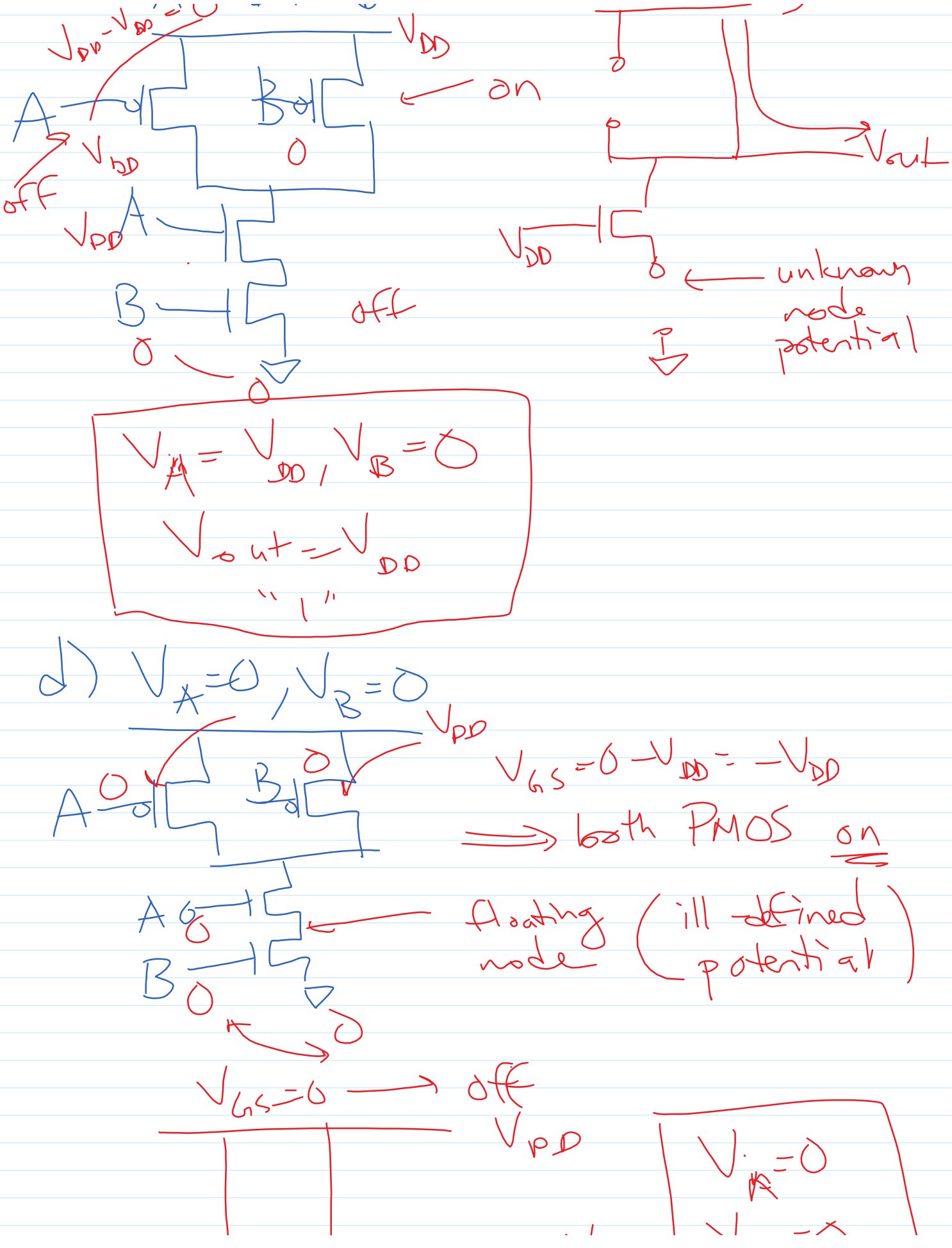


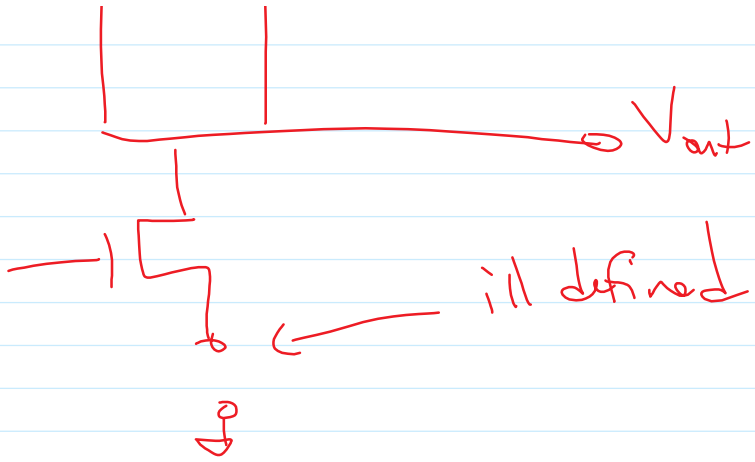

$V_A = 0$, $V_B = V_{DD}$

$V_{out} = V_{DD}$

c) $V_A = V_{DD}$, $V_B = 0$




$V_{DD}-V_{DD}=0$
$V_{DD}$
A
B
0
on
off
$V_{DD}$
$V_{DD}$
A
B
0
off
0
$V_A = V_{DD}$, $V_B = 0$
$V_{out} = V_{DD}$
"1"
$V_{out}$
$V_{DD}$
0
unknown node potential
I
d) $V_A = 0$, $V_B = 0$
$V_{DD}$
A
0
B
0
$V_{GS} = 0 - V_{DD} = -V_{DD}$
$\Rightarrow$ both PMOS on
A
B
0
floating node (ill-defined potential)
0
$V_{GS} = 0 \rightarrow$ off
$V_{DD}$
$V_A = 0$


$V_{out}$
ill defined
$V_B = 0$
$V_{out} = V_{DD}$