Discussion 1B Notes

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(Dated: June 29, 2020)

Discussion 1B notes for students taking EECS 16B during Summer Sessions 2020. Topics include: KVL, superposition, op-amps as comparators, op-amps in negative feedback.

I. KIRCHOFF'S VOLTAGE LAW (KVL)

Much like how Kirchoff's Current Law (KCL) follows from conservation of charge, Kirchoff's Voltage Law (KVL) follows from conservation of energy around a closed loop. Specifically,

$$\sum_{loop} V_i = 0$$

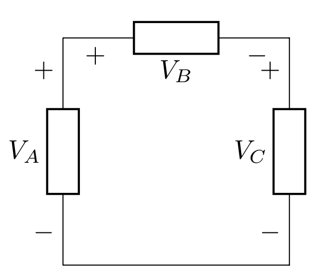
where the index i iterates through each circuit element in the loop.

Procedure 1 (Solving circuits with KVL):

1. Label each element with (+) and (-) signs.
2. "Walk around" the loop. To determine the sign of each voltage V_i, use the label you first encounter. If you first encounter a (+) sign, add the voltage; if you first encounter a (-) sign, subtract the voltage. Repeat for each independent loop.
3. Add additional constraints on the current using KCL.
4. Use I-V relations to write the equations in terms of known values.
5. Solve the system of equations using your favorite method.

Some remarks on this method:

1. Unlike the nodal analysis method, both KCL and KVL are explictly invoked in this method.
2. Regarding step 2, how many loops is enough loops? Roughly, I would say that you should draw enough loops such that each circuit element is included.
3. Regarding step 1, see the following figure for an example.

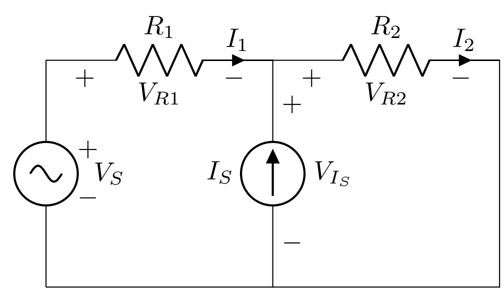


Let's say we draw a clockwise loop. Then the first sign we see is a (-) sign, so I add $-V_A$. The next element, we see a (+) sign first, so we add $+V_B$. Same for the next element, we add $+V_C$. In total:

$$-V_A + V_B + V_C = 0$$

If we had drawn a counterclockwise loop, the signs would have been flipped. However, in the end it becomes the same equation.

Example 1.1



1. **Label each element with (+) and (-) signs.** We have already done so on the diagram.
2. **For each loop, write a KVL equation.**
   (a) Loop 1: Pick the clockwise loop on the left half.
   $$-V_S + V_{R1} + V_{I_S} = 0$$
   (b) Loop 2: Pick the clockwise loop on the right half.
   $$-V_{I_S} + V_{R2} = 0$$
3. **Add constraints with KCL:** The junction of interest is the one where the two resistors and the current source meet.
   $$I_S + I_1 - I_2 = 0$$
4. **Use I-V relations to write equations in terms of knowns:** Ohm's law is all we need in this case.
   $$-V_S + I_1R_1 + V_{I_S} = 0$$
   $$-V_{I_S} + I_2R_2 = 0$$

5. **Solve the system of equations:** In this case, we have three equations and three unknowns: I_1, I_2, and V_{I_S}. Note that we can add the two loop equations in order to reduce the number of unknowns to just two, I_1 and I_2.

$$\begin{aligned} -V_S + I_1 R_1 + I_2 R_2 &= 0 \\ I_S + I_1 - I_2 &= 0 \end{aligned}$$

In matrix form:

$$\begin{bmatrix} R_1 & R_2 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_S \\ I_S \end{bmatrix}$$

Our final solution is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{-I_S R_2 + V_S}{R_1 + R_2} \\ \frac{I_S R_1 + V_S}{R_1 + R_2} \end{bmatrix}$$

II. SUPERPOSITION

Superposition is a powerful circuit solving technique that fundamentally relies on linearity. Recall that when using any of the circuit solving techniques we have gone over (e.g. nodal analysis), we end up with a system of equations $A\vec{x} = \vec{b}$

$$A \begin{bmatrix} u_1 \\ \vdots \\ u_n \\ i_1 \vdots \\ i_m \end{bmatrix} = \begin{bmatrix} V_{S1} \\ \vdots \\ V_{Sj} \\ I_{S1} \\ \vdots \\ I_{Sk} \end{bmatrix}$$

where $\vec{x}$ contains the node potentials and branch currents, and $\vec{b}$ contains the independent current and voltage sources.

If we squint at this matrix equation, we might notice that we can express $\vec{b}$ as a sum of simpler $\vec{b}_i$'s:

$$\begin{bmatrix} V_{S1} \\ \vdots \\ V_{Sj} \\ I_{S1} \\ \vdots \\ I_{Sk} \end{bmatrix} = \begin{bmatrix} V_{S1} \\ 0 \\ \vdots \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ V_{S2} \\ \vdots \\ 0 \end{bmatrix} + \dots$$

Each of these has its own associated solution:

$$\begin{aligned} A\vec{x}_{Vs1} &= \vec{b}_{Vs1} \\ &\vdots \\ A\vec{x}_{Vsj} &= \vec{b}_{Vsj} \\ A\vec{x}_{Is1} &= \vec{b}_{Is1} \\ &\vdots \\ A\vec{x}_{Isk} &= \vec{b}_{Isk} \end{aligned}$$

In effect, each solution contains the contribution of only one independent voltage or current source, with every other voltage or current source "zeroed out". By linearity, we can add these smaller solutions back together to obtain the solution to the original equation $A\vec{x} = \vec{b}$.

$$\vec{b} = \sum_i \vec{b_i} = A \sum_i \vec{x}_i = A\vec{x}$$

That was a lot of math, but it can summed up in the following procedure.

Procedure 2 (Superposition):

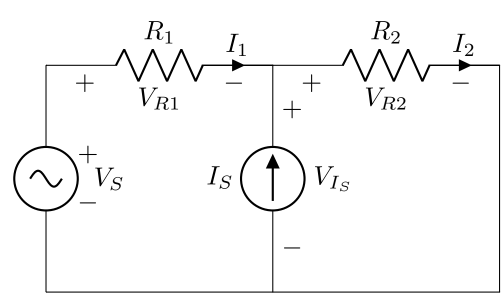
1. For a given independent source: "turn off" all other independent sources. Recall from Thevenin and Norton equivalent circuits that this means that a current source becomes an open circuit, and a voltage source becomes a wire.

2. Solve for the voltage(s) and/or current(s) of interest. **Maintain the same sign convention throughout.**

3. Repeat steps 1 and 2 for every independent source. At the end, sum the individual contributions together.

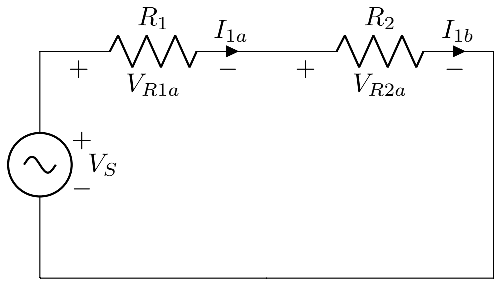
As an example, let's revisit Example 1.

Example 2.1



1. Voltage source V_S:

   (a) **Zero out every other independent source:** We convert the current source I_S into an open circuit.



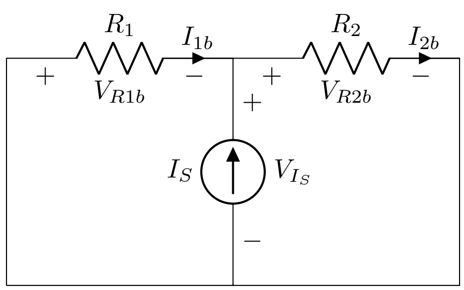
(b) **Solve the circuit:** To match what we did in Example 1, we solve for I_{1a} and I_{2a}.

$$I_{1a} = I_{2a} = \frac{V_S}{R_1 + R_2}$$

In this case, we used the equivalent resistance of resistors in series to simplify the analysis.

2. Current source I_S:

(a) **Zero out every other independent source:** We convert the voltage source V_S into a wire.



(b) **Solve the circuit:** This is a current divider circuit, which like the voltage divider has a solution that is worth memorizing.

From KCL:

$$I_{1b} + I_S = I_{2b}$$

From KVL, picking the loop only contain resistors:

$$V_{R1b} + V_{R2b} = I_{1b}R_1 + I_{2b}R_2 = 0$$

Solving this system of equations, we obtain:

$$I_{1b} = -I_S \frac{R_2}{R_1 + R_2}$$
$$I_{2b} = +I_S \frac{R_1}{R_1 + R_2}$$

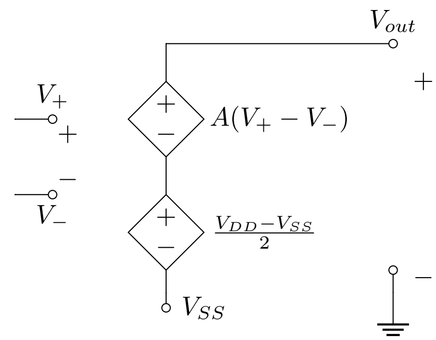
3. **Sum the individual contributions**:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} I_{1a} \\ I_{2a} \end{bmatrix} + \begin{bmatrix} I_{1b} \\ I_{2b} \end{bmatrix} = \begin{bmatrix} \frac{-I_S R_2 + V_S}{R_1 + R_2} \\ \frac{I_S R_1 + V_S}{R_1 + R_2} \end{bmatrix}$$

This matches our result from Example 1. Hurrah!

III. OPERATIONAL AMPLIFIERS (OP-AMPS)

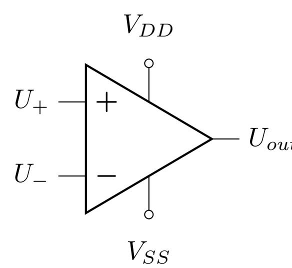
Operational amplifiers are a circuit component that amplify an input voltage difference. The internal structure and design of an op-amp is a topic that one can spend years studying (see EE105, EE140), but for the purpose of EECS16A and EECS16B, we model the op-amp as such:



Using KVL, we may ascertain the behavior of the op-amp:

$$-V_{out} + A(V_+ - V_-) + \frac{V_{DD} - V_{SS}}{2} + V_{SS} = 0$$
$$V_{out} = A(V_+ - V_-) + \frac{V_{DD} + V_{SS}}{2}$$

We sum up this internal circuit with this symbol:



where V_{DD} and V_{SS} are the power rails, V_+ and V_- are the input ports, and V_{out} is the output port. In total, an op-amp is a 5-terminal device!

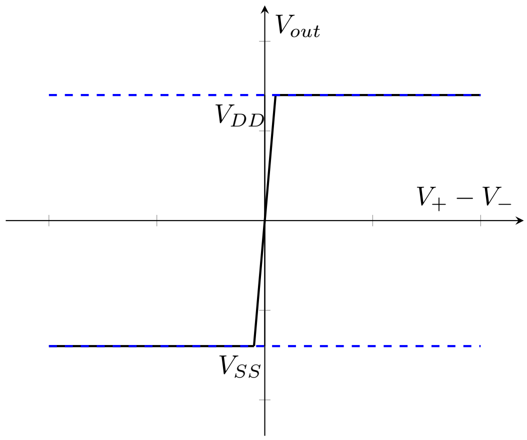
Let's look at the input-output behavior of the op-amp a little more closely. We note that the output is limited by the power rails, i.e. $V_{SS} \leq V_{out} \leq V_{DD}$. So really,

$$V_{out} = \begin{cases} V_{SS} & AV_{in} + \frac{V_{DD}+V_{SS}}{2} < V_{SS} \\ AV_{in} + \frac{V_{DD}+V_{SS}}{2} & V_{SS} \leq AV_{in} + \frac{V_{DD}+V_{SS}}{2} \leq V_{DD} \\ V_{DD} & AV_{in} + \frac{V_{DD}+V_{SS}}{2} > V_{DD} \end{cases}$$

where $V_{in} = V_+ - V_-$. If we pick the power rails such that $V_{DD} = -V_{SS}$, then we can simplify this expression:

$$V_{out} = \begin{cases} V_{SS} & AV_{in} < V_{SS} \\ AV_{in} & V_{SS} \leq AV_{in} \leq V_{DD} \\ V_{DD} & AV_{in} > V_{DD} \end{cases}$$

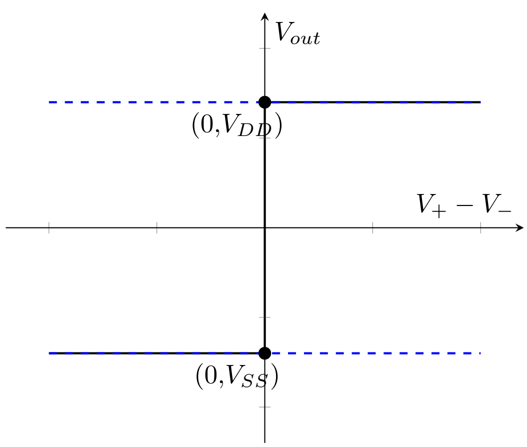
For moderate values of A, the plot is as follows:



Note that V_{DD} and V_{SS} have been chosen such that V_{out} is centered about 0 V, i.e. $V_{DD} = -V_{SS}$.

A. Op-Amps as Comparators

Op-amps are generally designed to have very large gains A. In the limit that A approaches ∞, the input-output curve starts approaching that of a step function, as in the following figure:



We might then think of an op-amp as a voltage "if-statement" of sorts.

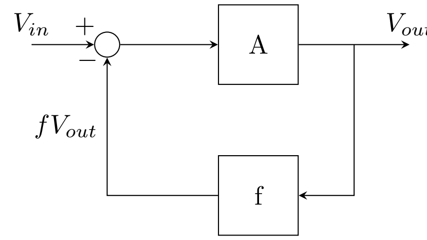
$$V_{out} = \begin{cases} V_{SS} & V_+ < V_- \\ V_{DD} & V_+ > V_- \end{cases}$$

In words, the op-amp *compares* V_+ and V_- and outputs a voltage depending on which is bigger. In this way an op-amp can be used as a **comparator**.

B. Negative Feedback

In practice, op-amps are not necessarily the best circuit to use as a comparator (the Wikipedia article on comparators has a good introduction to this topic). More commonly, op-amps are placed in **negative feedback**, which sacrifices gain for more predictable operation. We will see how negative feedback enables us to mainly operate in the linear regime of the op-amp, and how the transfer function (typically V_{out}/V_{in}) becomes determined by the external components in the feedback network as opposed to the specifics of the op-amp itself.

But first, what is negative feedback? In a feedback amplifier, some fraction f of the output is sent back to the input, and either added or subtracted. We distinguish between negative and positive feedback by the sign: if it is subtracted, the feedback opposes the original signal and is said to be negative (see below figure).

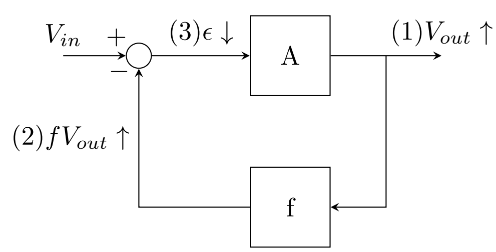


In this block diagram, A is the gain (sometimes called the *open-loop gain*, as it is what the gain would be with no feedback network) and f is the *feedback factor*. For most of the cases we will encounter in this class, $A > 0$ and $f > 0$. (More generally, the requirement for negative feedback would be that the *loop gain* Af is positive, but that is satisfied with $A > 0, f > 0$.)

Let's look at this block diagram a little more closely. The input to the gain block is the difference of V_{in} and fV_{out}, so

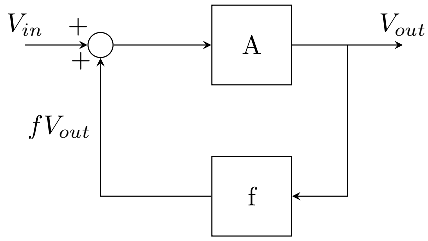
$$V_{out} = A(V_{in} - fV_{out})$$

Let's say the output is perturbed by some ΔV_{out}. Then $fV_{out} + f\Delta V_{out}$ is fed back and subtracted from V_{in}. But since $V_{out} = A(V_{in} - fV_{out}) - Af\Delta V_{out}$, we see that the output goes back down again! The negative feedback suppresses any change in the signal.



In the above block diagram, I have denoted the difference $V_{in} - fV_{out}$ as the *error signal* ϵ.

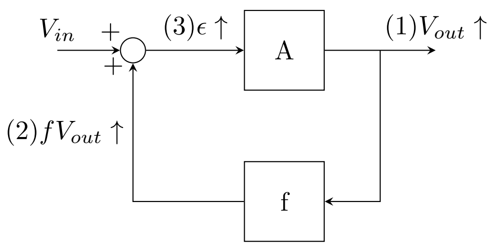
As a brief detour, let's consider the opposite case. If the feedback signal is added, the feedback magnifies any perturbations and is said to be positive (see below figure).



The output expression becomes

$$V_{out} = A(V_{in} + fV_{out})$$

Let us play the same game as before. We perturb the output signal by some ΔV_{out}. As before, $fV_{out} + f\Delta V_{out}$ is fed back. This time, however, the feedback signal is added to V_{in}, so we obtain $V_{out} = A(V_{in} + fV_{out}) + Af\Delta V_{out}$. We see that the output keeps growing, and that the positive feedback reinforces the perturbation.



In this case $\epsilon = V_{in} + fV_{out}$.

This method of perturbing the output and seeing which way the system responds (opposes? reinforces?) is in general how one should check for negative feedback.

C. Op-Amps in Negative Feedback

Before we place op-amps in negative feedback, let us assume we are working with ideal op-amps. In the EECS 16 series, that means that

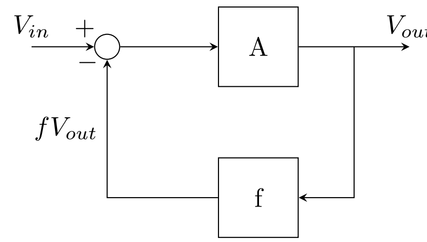
1. Input resistance is infinite.
2. Output resistance is zero.
3. Gain A is infinite.

Properties (1) and (2) are already captured in the circuit model we drew in this section's introduction. Property (1) means that the input terminals (+) and (+) lead to an open circuit. Property (2) means that no voltage is dropped between the output of the op-amp and any connections to other circuit elements, i.e. the node voltage V_{out} is indeed equal to $A(V_+ - V_-) + \frac{V_{DD}+V_{SS}}{2}$ instead of something like $A(V_+ - V_-) + \frac{V_{DD}+V_{SS}}{2} - IR_{out}$. Property (3) will have interesting implications for op-amps in negative feedback, which we now summarize in the so-called **"Golden Rules."**

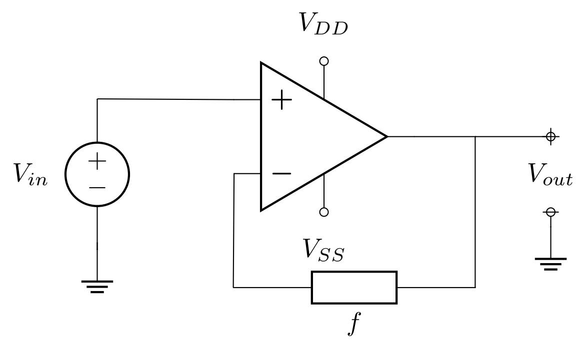
Golden Rules of Op-Amps

1. $I_+ = I_- = 0$. This follows from infinite input resistance. No current can flow into the input terminals of the op-amp if they lead to open circuits. This is always true for an ideal op-amp.
2. $V_+ = V_-$, **for an op-amp in negative feedback.** This golden rule follows from infinite gain, which we will now show.

Let us once again consider the block diagram from before:



Translating this to an op-amp in negative feedback:



So $V_+ = V_{in}$ and $V_- = fV_{out}$. Making the simplifying assumption that $V_{DD} = -V_{SS}$ so that the input-output relation exactly follows that of the block diagram,

$$V_{out} = A(V_+ - V_-) = A(V_{in} - fV_{out})$$

This can be solved for V_{out} in terms of V_{in}:

$$V_{out} = \frac{A}{1 + Af} V_{in}$$

Since $V_- = fV_{out}$

$$V_- = \frac{Af}{1 + Af} V_{in} = \frac{Af}{1 + Af} V_+$$

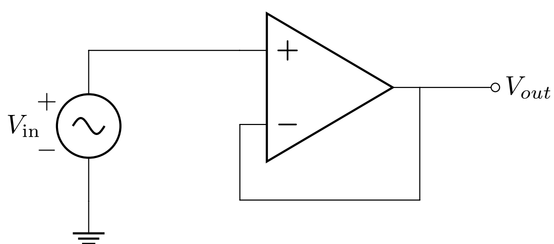
In the limit that $A \to \infty$, $V_- = V_+$.

The second golden rule might seem concerning – if $V_+ = V_- = 0$, then should the output always be zero, i.e. $V_{out} = A(V_+ - V_-) = A(0) = 0$? But as we will see when we go through a number of prototypical op-amp configurations, this is clearly not the case; the output is not a flat line at $V_{out} = 0$. Mathematically, this peculiarity can be resolved by the fact that we are multiplying ∞ by 0, and in the limit all sorts of wacky stuff can happen. Perhaps the above derivation can provide a more satisfying explanation: V_+ and V_- are not actually equal except in the limit of infinite gain; really, they are *almost* equal, with some finite but small error. This error is so small that when multiplied by the huge gain A, we are still operating in the linear regime of the op-amp, and thus we get out a finite output voltage. Indeed, no real op-amp would have infinite gain, so that is more akin to what is happening in the lab.

As a final note, many times when op-amps are connected in negative feedback, the power rails are omitted. This only makes sense for an op-amp connected in negative feedback, where it is assumed that the power rails are large enough such that we are always operating in the linear regime. The constraint that the output cannot exceed the power rails still holds however, so that is something that should be kept in the back of your mind.

D. Examples

Example 3.1 (Buffer/Voltage Follower)



The output is shorted to the inverting input, so

$$V_- = V_{out}$$

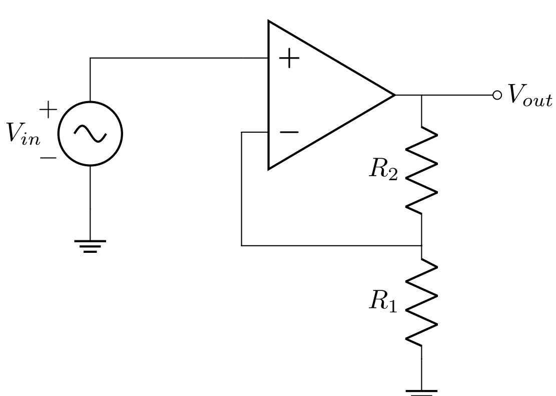
But by the second golden rule,

$$V_- = V_+$$

Thus, we have unity gain

$$V_{out} = V_- = V_+ = V_{in}$$

Example 3.2 (Noninverting Amplifier)



From the second golden rule,

$$V_- = V_+ = V_{in}$$

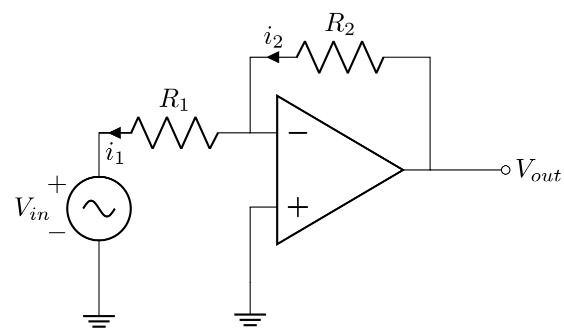
We could do KCL, but something of note is that since no current flows into the noninverting input of the op-amp, R_1 and R_2 form a voltage divider of V_{out}. Thus, we can jump immediately to our favorite voltage divider formula!

$$V_{in} = V_{out}\frac{R_1}{R_1 + R_2}$$

We want V_{out} in terms of V_{in} however, so we do a little switcheroo to get

$$V_{out} = (\frac{R_1 + R_2}{R_1})V_{in} = (1 + \frac{R_2}{R_1})V_{in}$$

Example 3.3 (Inverting Amplifier)



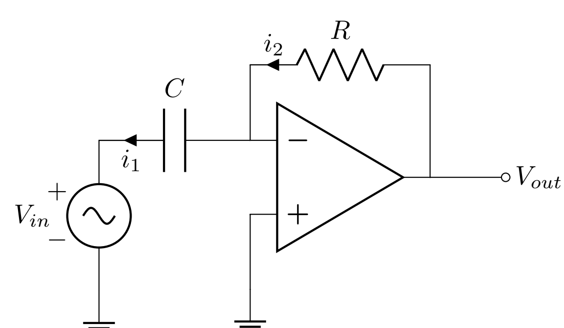
From KCL:

$$i_1 = i_2 \Rightarrow \frac{V_- - V_{in}}{R_1} = \frac{V_{out} - V_-}{R_2}$$

Note that we have implicitly invoked the Golden Rule #1, by not considering any currents flowing into the op-amp inputs. By Golden Rule #2, $V_+ = V_- = 0$. Thus,

$$V_{out} = -\frac{R_2}{R_1}V_{in}$$

Example 3.4 (Differentiator)



By KCL:

$$i_1 = i_2 \Rightarrow C\frac{d}{dt}(V_- - V_{in}(t)) = \frac{V_{out}(t) - V_-}{R}$$

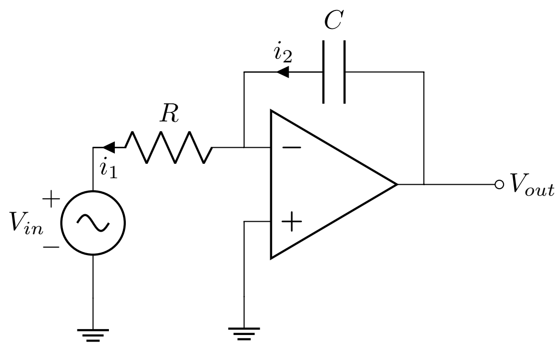
Plugging in $V_+ = V_- = 0$ by the second golden rule:

$$-C\frac{dV_{in}(t)}{dt} = \frac{V_{out}(t)}{R}$$

Thus, we see that this circuit takes a derivative of the input waveform!

$$V_{out}(t) = -RC\frac{dV_{in}(t)}{dt}$$

Example 3.4 (Integrator)



By KCL:

$$i_1 = i_2 \Rightarrow \frac{(V_- - V_{in}(t))}{R} = C\frac{d}{dt}(V_{out}(t) - V_-)$$

Plugging in $V_+ = V_- = 0$ by the second golden rule:

$$-\frac{V_{in}(t)}{R} = C\frac{dV_{out}(t)}{dt}$$

We obtain the differential equation

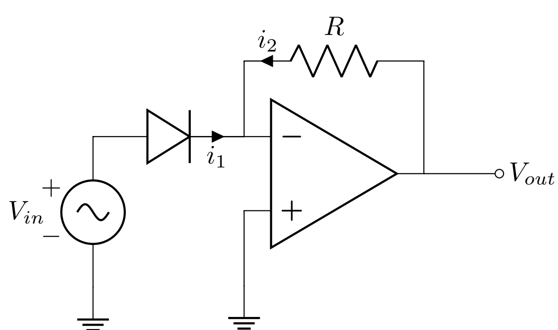
$$\frac{dV_{out}(t)}{dt} = -\frac{V_{in}(t)}{RC}$$

If we are given the initial condition $V_{out}(0)$ and would like to find the output at a time t_0:

$$V_{out}(t_0) = V_{out}(0) - \frac{1}{RC}\int_0^{t_0} V_{in}(t)dt$$

The output voltage changes over the time interval of interest by an amount proportional to the integral of the input signal!

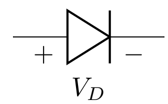
Example 3.5 (Exponential Amplifier)



We have introduced a new circuit element, the **diode**. Diodes are very interesting nonlinear circuit elements, which have the interesting property that they essentially only conduct current in one direction. For the purpose of this problem though, we invoke a more quantifiable version of their I-V behavior known as the Shockley Diode Equation:

$$I_D = I_S e^{\frac{qV_D}{k_B T}}$$

where V_D is defined as such:



The current equation is very intimidating looking, but suffice to say that I_S, q, and k_B are constants, and we will further assume that we are operating at a fixed temperature so that the temperature T is also a constant. The analysis is then essentially the same as the previous inverting-esque amplifier configurations, starting with KCL as usual.

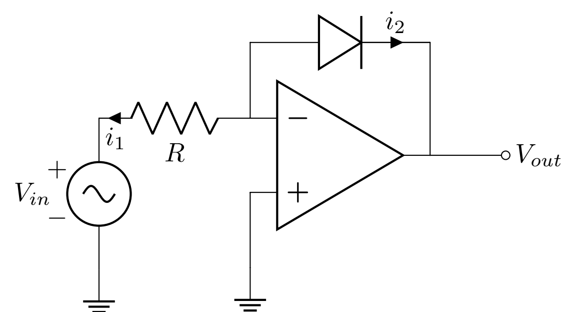
$$i_1 + i_2 = 0 \Rightarrow I_S e^{\frac{q}{k_B T}(V_{in} - V_-)} + \frac{V_{out} - V_-}{R} = 0$$

We have the same golden rule constraint, $V_- = V_+ = 0$, and thus:

$$V_{out} = -RI_S e^{\frac{qV_{in}}{k_B T}}$$

So the circuit exponentiates the input.

Example 3.6 (Log Amplifier)



From KCL:

$$i_1 + i_2 = 0 \Rightarrow \frac{V_- - V_{in}}{R} + I_S e^{\frac{q}{k_B T}(V_- - V_{out})} = 0$$

Plugging in the second golden rule and moving terms around:

$$V_{out} = -\frac{k_B T}{q}\ln\frac{V_{in}}{I_S R}$$

We see that operational amplifiers can do a myriad of mathematical operations, and in fact, before digital computers took over op-amps were a central component of analog computers.